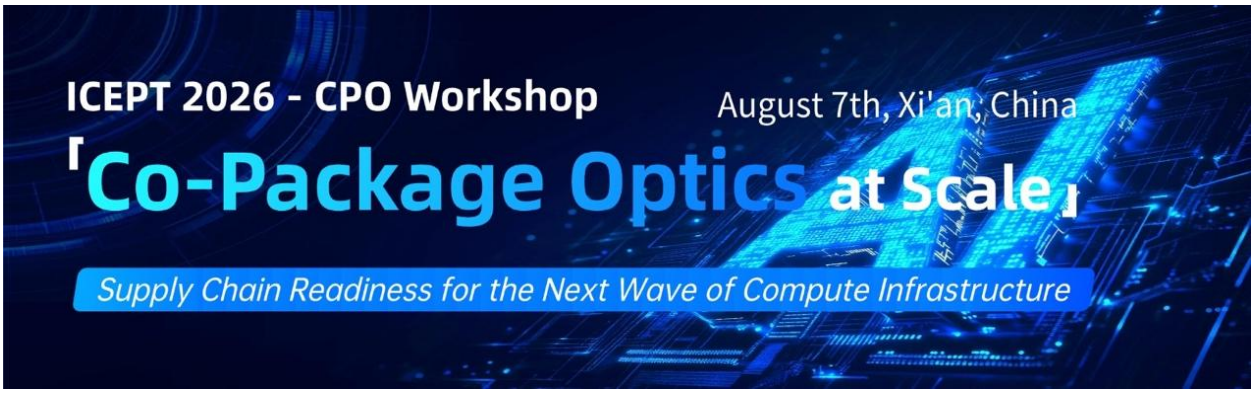


Date: August 7th, 2026, 08:30-12:35, Friday

Location: Xi'an, China. Hotel Wyndham Grand Xi'an South

Chair
Dr. Farhang Yazdani
CEO
BroadPak Corp.

Co-Chair
Dr. Qidong WANG
Director of Packaging and Integration R&D Center
Institute of Microelectronics, Chinese Academy of Sciences

Abstract:

Co-packaged optics (CPO) is widely recognized as a critical enabler for scaling bandwidth and energy efficiency in AI and hyperscale data center systems. However, beyond device innovation, the path to volume deployment is fundamentally a supply chain challenge. Unlike traditional pluggable optics, CPO requires deep integration across semiconductor, photonics, packaging, fiber attach, and system assembly ecosystems—introducing new dependencies, risks, and coordination requirements.

This workshop focuses on the emerging CPO supply chain and the structural shifts required to support high-volume manufacturing. We will examine how responsibilities are redistributed across foundries, OSATs, photonics providers, substrate vendors, fiber assembly houses, and system integrators. Key topics include supply chain fragmentation vs. vertical integration, alignment of yield models across heterogeneous components, known-good-die strategies, and the implications of integrating optical and electrical test flows.

Participants will explore bottlenecks such as laser sourcing (on-chip vs. external), fiber attach scalability, thermal interface materials, and advanced substrate availability. The session will also address logistics challenges including repairability, field service models, inventory risk, and standardization efforts that could enable multi-vendor interoperability.

A dedicated segment will examine the role of venture capital and private investment in accelerating the CPO ecosystem. We will explore how capital is being deployed across the value chain—from silicon photonics startups and laser integration technologies to advanced packaging and manufacturing automation—and how investment

trends are shaping technology roadmaps and supply chain consolidation. Discussion will include risk-return profiles, timing of scale inflection points, partnership models between startups and incumbents, and the strategic implications of capital concentration in critical supply nodes.

Through industry perspectives, investment insights, and case studies, this workshop will provide a holistic view of how supply chain maturity—not just technology readiness—will determine the pace and success of CPO adoption. Attendees will leave with a clearer understanding of where coordination is needed, where risks are concentrated, how capital is influencing the ecosystem, and what strategic decisions organizations must make to participate effectively in the CPO landscape.

Advance Program

	8:30-8:40 **Opening Remarks (Farhang Yazdani & Qidong Wang)**
	**8:40-8:55** **Photonic Packaging** *Yik Yee TAN* *Principal Market and Technology Analyst of Yole Group*
	**8:55-9:10** **Advanced Organic Substrates enabling co-package optics at scale** *Bula Wang* *TDI Director of AT&S*
	**9:10-9:25** **Material Technologies Enabling Co-Packaged Optics: Challenges and Solutions in Electronic-Photonic Hybrid Integration** *Yasuharu Murakami* *Senior Director of Resonac Corporation*
	**9:25-9:40** **Innovative Materials for Next-Gen Package Substrates and Co-Packaged Optics (CPO)** *Habib Hichri* *EVP, Senior Fellow, Global Applications and Business Development, Ajinomoto Fine Techno USA Corporation*
	9:40-10:15 **Panel Discussion**
10:15-10:50 Break	
	10:50-10:55 **Session Introduction (Farhang Yazdani & Qidong Wang)**

	**10:55-11:10** **Breaking the Laser Bottleneck: Simplifying Co-Packaged Optics Manufacturing with 60× Fewer DFB Lasers** *Pirooz Hojabri* *CEO of IC Photonics*
	**11:10-11:25** **Intelligent manufacturing solutions for advanced CPO, LPO, NPO & OCS** *Alex Cao* *G.M. of ficonTEC China*
	**11:25-11:40** **Challenges and Opportunities on Co-Packaged Optics Thermal-Mechanical Performance Towards High-Volume Ramping** *Shaw Fong Wong* *Principal Engineer & Engineering Director, Intel Corporation*
	11:40-12:20 **Panel Discussion**
12:20-13:30 Lunch	

Introduction of Speaker

Chair

Farhang Yazdani, CEO, BroadPak Corporation

BIO: Farhang Yazdani is a semiconductor executive, inventor, investor, author, and technology strategist with more than two decades of industry experience. He has played a pivotal role in advancing next-generation semiconductor packaging technologies, heterogeneous integration, chiplet architectures, silicon photonics, and co-packaged optics.

Farhang is the Founder and CEO of BroadPak Corporation and inventor of the groundbreaking 3DHI HiRise Packaging Technology. He is widely regarded as one of the industry's foremost experts in advanced packaging and 3D heterogeneous integration. He has authored numerous technical publications, holds more than 40 issued and pending patents, and has contributed extensively to the commercialization of innovative packaging technologies adopted throughout the global semiconductor ecosystem. He is the author of "Foundations of Heterogeneous Integration: An Industry-Based 2.5D/3D Pathfinding and Co-Design Approach", a widely respected reference book on advanced semiconductor integration and system-level co-design methodologies.

Farhang is a frequent keynote speaker, an industry advisor, and lecturer for the United States Patent and Trademark Office (USPTO). He has presented, chaired, and served as General/Technical program chair at major global conferences, including IEEE ECTC, ICEPT, ICEP, DAC, DATE, IMAPS, IEEE BUSS, and OIP. Farhang serves as the Co-Chair of the IMAPS Silicon Valley Chapter and contributes actively to industry roadmaps, technical committees, and professional development initiatives. He also serves on the Boards of Directors and Advisory Boards of several technology companies. He is the recipient of the NIPSIA Award for his significant contributions to semiconductor packaging innovation and technology advancement.

Chair

Qidong WANG, Director of Packaging and Integration R&D Center at the Institute of Microelectronics of the Chinese Academy of Sciences

BIO: Dr. WANG Qidong received his B.S. degree in Electronics Engineering from Southeast University in Nanjing, MSC degree from Nottingham University in UK, Ph.D degree in Microelectronics and Solid-State Electronics from University of Chinese Academy of Sciences. He worked in Varian Lab, Stanford University as a Visiting Scholar from 2015 to 2016. He currently serves as the Director of Packaging and Integration R&D Center in the Institute of Microelectronics of the Chinese Academy of Sciences. Dr. Wang has served ICEPT as session chair nearly 10 years, as technical chair since 2023-present.

Yik Yee TAN, Principal Market and Technology Analyst, Yole Group

BIO: Yik Yee (YY) Tan Ph.D. is a Principal Technology & Market Analyst, Semiconductor Packaging & Assembly at Yole Group. Dr. Tan holds a Ph.D. in Engineering from Multimedia University (MMU, Malaysia). She has more than 25 years of experience in semiconductor packaging. Based on her technical expertise and market knowledge, she develops technology & market reports and is engaged in dedicated custom projects. Prior to Yole, Dr. Tan worked as a failure analyst and interconnect champion at Infineon Technologies (Malaysia) and later as an open innovation senior manager at Onsemi (Malaysia).
She published more than 30 papers and hold 4 patents and award winner for IEEE EPS - Regional 10 Contribution Award 2024 and IEEE Malaysia Section – Outstanding Industry Volunteer Award 2024. Adjunct Professor at Nottingham Malaysia

Speech Title/ Abstract: **Photonic Packaging**

The exponential growth of data-intensive applications, including artificial intelligence (AI), high-performance computing (HPC), and hyperscale data centers, is driving unprecedented demand for higher bandwidth, improved energy efficiency, and lower latency interconnects. Traditional electrical interconnects are approaching their physical and power limits, positioning photonic integration as a key solution. Photonic packaging plays a critical role in enabling this transition by integrating photonic integrated circuits (PICs) with electronic integrated circuits (EICs), bringing optical interconnects closer to compute engines.
A central theme in this domain is heterogeneous integration of PICs and EICs, where advanced packaging technologies allow the co-integration of optics and electronics within a unified platform. Approaches such as 2.5D interposers, fan-out packaging, and 3D stacking are increasingly adopted to support this integration. Industry developments highlight the diversity of architecture from TSMC's COUPE, ASE FOCoS and other emerging solutions.
This presentation will focus on the market trends, technology trends and the challenges of photonic packaging. How the transition reshapes the supply chain, opportunity for OSATs, and also driving new partnerships across the photonics and semiconductor ecosystems.

Bula Wang, TDI Director, AT&S

BIO: Bula Wang, as the Director of Technology Development for AT&S Microelectronics Business Unit, is responsible for leading and managing engineering solutions for ABF substrate products. He has more than 20 years of extensive experience in the advanced packaging field, including OSAT and ABF substrates manufacturers. Prior to joining AT&S, Bula worked for ASE and Access for R&D and technical role.

Speech Title/ Abstract: **Advanced Organic Substrates enabling co-package optics at scale**

High speed data infrastructure with very high efficiency is necessary to meet the demands of increasing AI workloads, next generation datacenters and HPC. Several industrial leading companies are working on CPO to reap performance benefits like reduced power, low latency and improved signal integrity. With these increasing architectural complexities and innovative approaches in advanced packaging, IC substrates have also evolved overtime to meet the market trends and demands. This talk focuses on how IC substrates play a crucial role in addressing CPO manufacturing, performance and functionality challenges.

Yasuharu Murakami, Yasuharu Murakami, Resonac Corporation

BIO: Yasuharu Murakami is Senior Director of the Research Institute Strategy Department at Resonac Corporation. He received a Ph.D. in Engineering from the Institute of Science Tokyo and has over 20 years of experience in the development of electronic materials such as dry film resists, photodefinable redistribution materials, and transparent display materials.

Speech Title/ Abstract: **Material Technologies Enabling Co-Packaged Optics: Challenges and Solutions in Electronic-Photonic Hybrid Integration**

With the rapid expansion of AI and data-center demand, semiconductor packaging must achieve significant advancements in bandwidth, power efficiency, and integration density. Co-Packaged Optics (CPO) is attracting attention as an optical interconnect technology that replaces electrical interconnects and requires advanced integration of electronics and photonics.

This presentation outlines the requirements and challenges of hybrid integration in advanced electronic-photonic packaging, focusing on key technical issues in the optical engine domain, including optical path design, coupling,

assembly precision, thermal management, and reliability. It also presents our material technology developments, including polymer waveguides, optical adhesives, and thermal management materials.

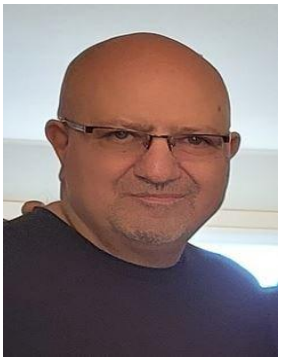
Habib Hichri, EVP, Senior Fellow, Global Applications and Business Development, Ajinomoto Fine Techno USA Corporation

BIO: Habib Hichri is Executive Vice President and Senior Fellow for Global Applications and Business Development at Ajinomoto Fine-Techno USA. Previously, he was Director of Applications Engineering at SUSS MicroTec Photonics Systems USA, providing patterning solutions for advanced semiconductor packaging. He spent 12 years at IBM's Semiconductor R&D Center in East Fishkill, NY, as lead process integration engineer and later in management for front-end microprocessor fabrication. Habib holds over 40 U.S. patents, has authored 75+ publications, and contributed a book chapter to Advances in Embedded and Fan-Out Wafer Level Packaging Technologies (Wiley-IEEE). He earned his Master's and PhD in Chemical Engineering from Claude Bernard University, France, and an MBA from SUNY Buffalo. Chair of IEEE/EPS Orange County, he serves on ECTC and IMAPS committees, is an IMAPS Fellow, and sits on the IMAPS Executive Council. Since 2024, he has been a board member of iNEMI and, since 2025, of the International Semiconductor Industry Group (ISIG).

Speech Title/ Abstract: I**nnovative Materials for Next-Gen Package Substrates and Co-Packaged Optics (CPO)**

Advanced semiconductor packages require insulating and optical-interconnect materials that deliver high reliability, low transmission loss, and compatibility with dense multilayer fabrication. Ajinomoto Build-up Film™ (ABF™) is widely used for package substrates because of its insulation reliability, thickness uniformity, and suitability for semi-additive processes.

This presentation introduces ABFT and discusses polymer optical waveguides and adhesive materials for co-packaged optics (CPO), highlighting their potential to support lower power consumption, higher bandwidth density, thermal stability, robust bonding, and standard substrate-process compatibility.



Pirooz Hojabri, CEO of IC Photonics

BIO: Pirooz Hojabri is a seasoned technology executive with more than 40 years of leadership experience spanning RF systems, mixed-signal ASICs, digital signal processing (DSP), and silicon photonics. A named inventor on 11 patents, he has led the development and commercialization of innovative technologies while holding senior leadership roles at industry-leading companies including IPG Photonics, Lumentum, Texas Instruments, Tektronix, Plato Networks, and National Semiconductor.

Speech Title/ Abstract: **Breaking the Laser Bottleneck: Simplifying Co-Packaged Optics This presentation** introduces a highly scalable External Laser Source (ELS) architecture that simplifies co-packaged optics (CPO) by reducing distributed DFB laser count by approximately 60×. The centralized laser architecture alleviates supply chain constraints while improving manufacturability, yield, reliability, and total cost of ownership through built-in redundancy and simplified system design.

The significant reduction in laser count also enables cost-effective WDM deployment and higher optical launch power, improving end-to-end PAM4 link performance and achieving 10^{-14} BER without forward error correction (FEC). Eliminating FEC reduces both latency and power consumption, enabling faster, more efficient data movement between compute and memory. By increasing bandwidth density, improving energy efficiency, and enhancing system resilience, this architecture provides a practical pathway for scaling next-generation AI networking while addressing one of the industry's greatest challenges—the widening gap between compute performance and memory access.

Alex Cao, G.M. of ficonTEC China

BIO: Alex Cao is the General Manager of ficonTEC China, based in Shanghai, China. He holds a master's degree in information technology and brings more than 30 years of industry experience spanning both semiconductor and photonics technologies.

Alex has over 10 years of experience in the semiconductor industry, specializing in IC testing and burn-in solutions. In addition, he has more than 20 years of experience in photonics, with a strong focus on automation systems and optical components for telecommunications, datacom, and high-power diode laser (HPDL) applications.

Since joining ficonTEC in 2003, Alex has played a key role in establishing and expanding the company's presence in China. Under his leadership, ficonTEC China has grown from a small sales office into a full-fledged organization with capabilities in engineering, system design, assembly, service, and customer support.

With his extensive expertise in automation, photonics manufacturing, and market development, Alex continues to drive ficonTEC's growth and innovation in the Chinese market.

Speech Title/ Abstract: Intelligent manufacturing solutions for advanced CPO, LPO, NPO & OCS

The explosive growth of AI infrastructure and hyperscale data centers is accelerating the adoption of next-generation optical interconnect technologies, including Co-Packaged Optics (CPO), Linear Pluggable Optics (LPO), Near-Packaged Optics (NPO), and Optical Circuit Switching (OCS). While these technologies enable higher bandwidth, lower power consumption, and improved system scalability, they also introduce new manufacturing challenges that demand greater precision, automation, and production flexibility.

This presentation explores intelligent manufacturing solutions that enable the transition from prototype development to high-volume manufacturing (HVM) for advanced optical packaging and interconnect products. Key manufacturing challenges—including precision active alignment, automated assembly, scalable testing, yield optimization, process migration, and quality assurance—will be discussed, along with strategies for minimizing manual intervention while maintaining high throughput and consistent product quality.

Shaw Fong Wong, Principal Engineer & Engineering Director, Intel Corporation

BIO: Dr. Shaw Fong Wong serves as the IEEE Electronic Packaging Society (EPS) Region 10 Program Director, where he drives regional IEEE initiatives in semiconductor packaging, talent development, and industry-academia collaboration across Asia-Pacific. He is also an active Exco Members of the IEEE Malaysia Section, contributing to industry relations and ecosystem engagement. Dr. Wong is a registered Professional Engineer (Ir.) with the Board of Engineers Malaysia (BEM) and currently serves as an Industry Advisory Panel (IAP) member to leading universities, including University of Malaya, Universiti Malaysia Perlis, and Xiamen University Malaysia, supporting curriculum development aligned with industry needs. He is an elected Fellow of the ASEAN Academy of Engineering and Technology (AAET). With a Ph.D. in electronic packaging, Dr. Wong has authored over 100 technical publications and holds 14 patents and trade secrets. He is currently a Principal Engineer and Engineering Director at Intel Malaysia, based in Kulim, Kedah, with over 25 years of experience in semiconductor technology and advanced packaging.

Speech Title/ Abstract: **Challenges and Opportunities on Co-Packaged Optics Thermal-Mechanical Performance Towards High-Volume Ramping**

Co-Packaged Optics (CPO) is widely viewed as a key technology for enabling the bandwidth density and energy efficiency required by AI, high-performance computing, and next-generation data centre infrastructure. As the industry moves from prototype demonstrations to volume deployment, thermal-mechanical performance is becoming a critical determinant of manufacturability, yield, reliability, and supply chain scalability.

This discussion will cover key thermal-mechanical challenges associated with integrating silicon/optical engines, advanced substrates, and fibre assemblies within a single package. Topics include thermal coupling between optical

and electrical components, package warpage control, fibre attach robustness, thermo-mechanical stress management, and field reliability considerations. The impact of these challenges on assembly yield, known-good-die strategies, repairability, and manufacturing readiness will also be examined.
The presentation will further explore opportunities together on reliability-aware manufacturing practices, providing a platform to discussion on accelerating CPO adoption toward high-volume production.

Cheng YANG, Industry Expert

BIO: Dr.Yang has more than 26 years' experience in electronics system and IC packaging development. As the industrial expert, he has worked at Flex on SiP products and technology development in IoT, automotive, medical, and industrial applications, covering design, manufacturing, and testing areas. He has worked at Intel on memory packaging design and technology development for 13 years. Dr. Yang hold a Ph.D. degree from National University of Singapore, EMBA from Washington University in St. Louis, and Master and Bachelor from Shanghai Jiaotong University.

Scott CHEN, Sr. VP of Central Developing Engineering, ASE Group, Chung-Li

BIO: Scott received B.S. degree in Chemical Engineering from NTU (National Taiwan University). And Master degree of Executive MBA Program from NTU. He has been worked on each of assy technology , MEMS nsor, bumping, flip chip , advance package technology and SIP solution over 30 yrs.

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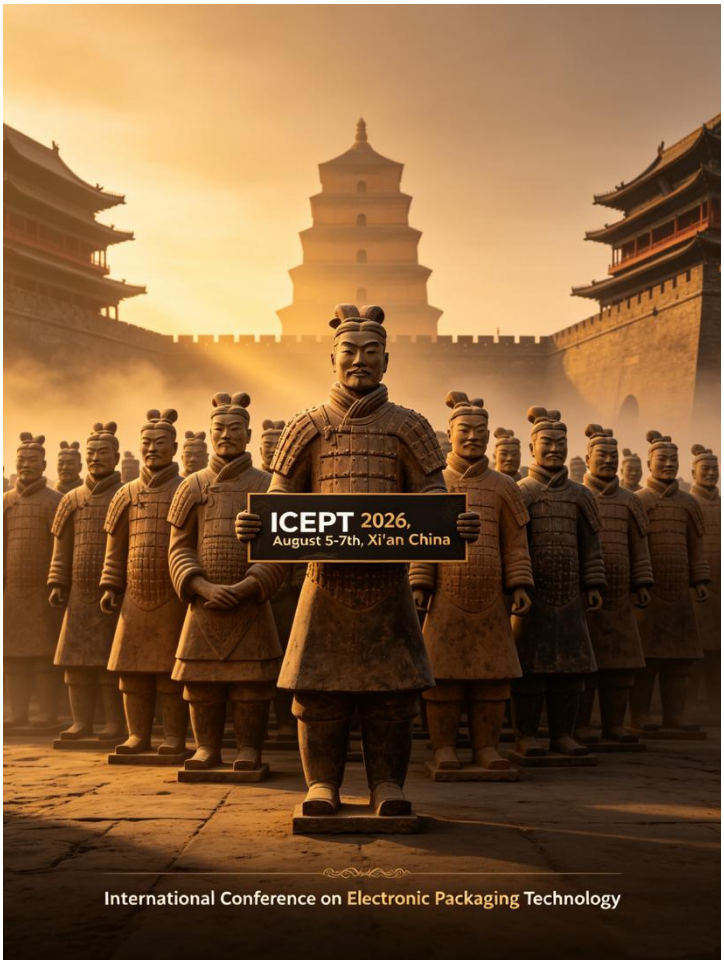
Contact: Secretary: Janey SHI, Janey@fsemi.tech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