

August 5-7th, Xi'an China

ICEPT 2026 Program Overview

August 5 th	Time	Room 1		Room 2		Room 3		Room 4	
	8:30-12:05	PDC 1-2		PDC 3-4		PDC 5-6		PDC 7-8	
	13:00-16:15	Special Session 1-2		Special Session 3-4		Special Session 5-6		Special Session 7-8	
	20:30-22:30	EPS Cup · Football Game							
August 6 th	8:30-12:10	Plenary 1-5							
		Room 1	Room 2	Room 3	Room 4	Room 5	Room 6	Room 7	Room 8
	13:00-15:10	Session 1	Session 2	Session 3	Session 4	Session 5	Session 6	Session 7	Session 8
	15:10-15:50	Poster Session A							
	15:50-18:00	Session 9	Session 10	Session 11	Session 12	Session 13	Session 14	Session 15	Session 16
	18:30-21:00	Welcome Dinner							
August 7 th		Room 1	Room 2	Room 3	Room 4	Room 5	Room 6	Room 7	Room 8
	08:30-10:10	Session 17	Session 18	Session 19	Session 20	Session 21	Session 22	Session 23	Session 24
	10:10-10:50	Poster Session B							
	10:50-12:30	Session 25	Session 26	Session 27	Session 28	Session 29	Session 30	Session 31	Session 32
	13:30-15:30	Plenary 6-9							
	15:30-16:10	Poster Session C							
	16:10-18:10	Plenary 10-13							
	END								



August 5 th AM --- Professional Development Course				
Time	Room 1	Room 2	Room 3	Room 4
8:30-10:10	PDC 1 - Driving the megawatt AI Era: Next-Gen packaging	PDC 3 - Advanced System Packaging and Solder Interconnection	PDC 5 - Cu-Cu Hybrid Bonding and Co-Packaged Optics with Silicon Photonics	PDC 7 - Photonic Components and Packaging Technologies for Optical Links
	<i>Mr. Scott CHEN</i> ASE Group	<i>Dr. Way Koh, Jusheng MA</i> Pacrim Technology, Tsinghua University	<i>Dr. John LAU</i> Unimicron Technology Corporation	<i>Dr. Torsten Wipiejewski</i> Huawei Technologies Duesseldorf GmbH
10:10-10:25	Break			
10:25-12:05	PDC 2 - Nano Materials and Polymer Composites for Electronic Packaging	PDC 4 - High Reliability Soldering in Semiconductor Packaging	PDC 6 - Wafer Bonding and Hybrid Bonding Technologies: From Fundamentals to Frontier Applications	PDC 8 - Experimental Methods for Stress and Strain Analysis of Advanced Electronics Packaging
	<i>Prof. Zhuo LI</i> Fudan University	<i>Dr. Ningcheng LI</i> IEEE Fellow	<i>Prof. Chenxi WANG</i> Harbin Institute of Technology	<i>Prof. Jeff Suhling</i> Auburn University
12:05-13:00	Break			



August 5 th PM --- Special Sessions				
Time	Room 1	Room 2	Room 3	Room 4
Special Session	1-IEEE-EPS R10 Interactive Session	3-EDA for AP & System Integration Empyrean 华大九天	5-Hybrid Bonding Technology	7- Digital Lithography Technology Forum: Advanced Packaging and Micro/Nano Devices CFMEE 芯基微装
Chair	<i>Prof. Qian WANG, Chair of IEEE-EPS Beijing Chapter</i>	<i>Prof. Jun YANG, Southeast University</i>	<i>Dr. Kenny YE, Senior Vice President of Piotech, Inc.</i>	<i>Dr. Wenhui MEI, CFMEE</i>
13:00-14:25	<i>Prof. Jeffrey C. Suhling, Dr. Shaw Fong Wong, IEEE EPS</i>	<i>Address</i>	<i>Address</i>	<i>Address</i>
	Right-sized AI at the Edge: Scaling Intelligence with Big Impact <i>Dr. Poh Leng EU, NXP Semiconductors</i>	Bridging PCB and Advanced Packaging: Our Journey Toward Package-Aware Design <i>Mr. Liang JIA, Huatek</i>	Low Distortion Wafer Bonding using programmable wafer deflection for advanced semiconductor manufacturing <i>Dr. Li GONG, General Manager, SUSS MicroTec (Shanghai) LTD</i>	Developments and Trends in Digital Lithography <i>Dr. Wenhui MEI, Chief Scientist, Keenovo Microelectronics</i>
	The Second Wave of PLP for HPC and AI Applications <i>Dr. Tanja Braun, Fraunhofer IZM</i>	Advanced Packaging Design & Simulation Solutions and Challenges <i>Mr. Guangchao LV, NCAP</i>	Trends in Bonding Technology Driven by the AI Era <i>Mr. Ren Chaoqun, General manager, Wisdom SemiTeC (Jiangsu) Technology Co.,Ltd.</i>	Digital Lithography Enabling AI Chips and Advanced Packaging: Innovations and Breakthroughs in Domestic Equipment <i>Mr. Zhihong CAI, Product Manager, Keenovo Microelectronics</i>



	The Impact of The Dynamic AI Market on the Advanced Packaging Supply Chain <i>Dr. Yu-Po, Wang, Prismark</i>	Trends and Industrial Practices of STCO-Driven 3DIC Design Methodology <i>Dr. Michael LIU, Empyrean Technology Co., Ltd</i> Technology & Fusion, enabling AI innovation	Technology & Fusion, enabling AI innovation <i>Mr. Norito Matsumura, Senior Director, Tokyo Electron</i>	Advanced Packaging: From MEMS to Nanofabrication <i>Prof. Zewen LIU, School of Integrated Circuits, Tsinghua University</i>
14:25-14:35	Break			
Special Session	2-EPS R10 Session	4-EDA for AP & System Integration	6-Hybrid Bonding Special Session	8- Digital Lithography Technology Forum: Advanced Packaging and Micro/Nano Devices
Chair	<i>Prof. Huaiyu YE, Vice Chair of IEEE-EPS Guangzhou Chapter</i>	<i>Xiaoming LIU, Empyrean</i>	<i>Dr. Qidong WANG, IMECAS</i>	<i>Dr. Wenhui MEI, CFMEE</i>
14:35-16:15	TBD <i>Mr. Kazuyuki Nakagawa, General Chair of ICSJ 2026</i>	Physically Aware Logic Synthesis in the AI Era <i>Prof. Keren ZHU, Fudan University</i>	Plasma Activation in the Downstream Region of a Surface-Wave-Excited Plasma for Hybrid Bonding <i>Dr. Yasuhiro Morikawa, Technology Manager (Global Technology Sensing Strategy), ULVAC, Inc.</i>	Digital Lithography-Enabled Solutions for Diverse Research Applications <i>Mr. Weilong CHEN, Product Manager, Keenovo Microelectronics</i>

	QULET: Quantum Chiplet Integration Technology for Superconducting Quantum Computing <i>Jiexun YU, Tsinghua University</i>	EDA Co-Simulation and Optimization of Structural Reliability for Full Lifecycle: Chip Design, Packaging, System Integration and Reliability Test <i>Dr. Jian CHENG, JCET</i>	The Next 3D Frontier: Equipment Perspectives on D2W Hybrid Bonding Challenges <i>Mr. Jonathan Abdilla, Director Technology, Besi</i>	Advanced Packaging for the AI Era <i>Dr. Zhengda WU, Deputy General Manager, Payton Technology</i>
	Panel <i>Chair: Prof. Zhuo LI, Chair of IEEE-EPS Shanghai Chapter</i> Interactive Panel Panelist: Jeff Suhling, Shaw Fong Wong...	Thermal Simulation of Chiplet heterogeneous Integration system <i>Dr. Qinzhi XU, IMECAS</i>	Fusion & Hybrid Bonding: Driving Application Performance, Power and Cost by Mixing and Matching Semiconductor Technologies <i>Mr. Thomas Pleschke, Business Development, EV Group (EVG)</i>	/
		Panel	Pushing The Limit of Bonding Accuracy and Throughput <i>Mr. Bin ZHAO, iSTAR</i>	/
20:30-22:30	EPS Cup · Football Game			



August 6 th AM --- Plenary Talk	
Opening Ceremony	
Chair	<i>Prof. Kouchi ZHANG, Academician of the Netherlands Academy of Engineering</i>
08:30-08:45	Welcome Address
	<i>Prof. Tianchun YE, Chair of ICEPT, China</i>
	<i>Prof. Xiaohong GUAN, Xijiao University, China</i>
	<i>Prof. Jeffrey C. Suhling, IEEE EPS President, USA</i>
08:45-09:25	CP Wong Global Electronic Packaging Award 2026
	<i>Chair: Prof. Ricky LEE, Hong Kong University of Science and Technology (Guangzhou), China</i>
Plenary Talk	
09:25-09:55	Stress Sensing Test Chips for Application to Electronics Packaging
	<i>Prof. Jeffrey Suhling, IEEE EPS President, Auburn University, USA</i>
09:55-10:25	Heterogeneous and Hybrid Integration Technologies for the Era of Humanoid Robotics and the Low-Altitude Economy
	<i>Prof. Sheng LIU, Wuhan University, China</i>
10:25-10:40	Break & Exhibition
Chair	<i>Prof. Ricky LEE, Hong Kong University of Science and Technology (Guangzhou), China</i>
10:40-11:10	Sinterconnects® as a Platform for Double-Sided-sintered WBG Power Modules
	<i>Dr. Ali Roshanghias, Silicon Austria Labs (SAL), Austria</i>
11:10-11:40	Glass Packaging and Its Reliability
	<i>Dr. John H Lau, Unimicron Technology Corporation, USA</i>
11:40-12:10	Application Practice and Prospect of Advanced Packaging Technology for Intelligent Computing Chip System
	<i>Dr. Daohong Yang, Director of Yangtze Laboratory, Dean of the School of Integrated Circuits, Hubei University</i>
12:10-13:00	Lunch



August 6th PM Technical Sessions

Session	Room 1	Room 2	Room 3	Room 4
	Session 1	Session 2	Session 3	Session 4
	Manufacturing of Packaging Interposer	Polymeric Dielectrics and Adhesive Materials	Analysis of Packaging Reliability	Interconnect Design and Manufacturing Technologies
Committee	Track 1-1-Advanced Packaging	Track 2-1-Packaging Materials & Processes	Track 3-1-Packaging Design & Modeling	Track 4-1-Interconnection Technologies
Chairs	Daowei WU, The 771st Research Institute, CASC Shuye ZHANG, Harbin Institute of Technology	Tao HANG, Shanghai Jiaotong University Leidang ZHOU, Xijiao University	Xu LONG, Northwestern Polytechnical University Daoguo YANG, Guilin University of Electronic Technology	Yongjun HUO, Beijing Institute of Technology Shuying MA, Huatian Technology
13:00-13:25 Invited	Digital Lithography for Advanced Interconnects Toward-Zero-Compromise: Performance & Yield Co-Optimization Mr. Kazuya Aoki, USHIO INC., Japan	A Review of a Bi-free In-containing Lead-free Mid-temperature Solder Dr. Hongwen ZHANG, Indium Corporation, USA	Moldex3D Advanced Packaging Molding Analysis Solution and Latest Technological Advancements Dr. Leo Shen, CoreTech System Co., Ltd. (Moldex3D), China	Advances in Room-Temperature Surface-Activated Bonding for Heterogeneous Optoelectronic Integration Prof. Ryo Takigawa, Kyushu University, Japan
Oral 13:25-15:10	<68> Process-Integrated Co-Optimization(PICO) of Etch Profile and Metal Fill for Nano Through-Silicon Via (nTSV) Fabrication	<178> Multi-Objective Prediction and Discovery of High-Performance Polymer Dielectrics for Advanced Packaging	<233> Connectivity and thermal transport in porous sintered silver: A statistically controlled 2D-3D comparison	<30> Ion migration and dendrite growth in electrochemical migration failure of copper wires in printed circuit boards
	<763> SAFO Packaging Technology	<517> Through-silicon via (TSV) filling with polymeric materials; a comparison study	<525> Layout Optimization of Solder Ball Array for Fatigue Life Enhancement in Board-Level Radar Packages by FEA	<94> Sequential Plasma-activated low-temperature direct Ru-Ru bonding for ultrahigh density interconnection
	<236> A Parasitic Error Self-Compensating ZTT Nano-Alignment Device for Advanced Packaging	<152> Reliability Regulation of Solder Resist Materials for FCBGA via Rigid/Flexible Alkali-Soluble Resin Blending	<72> Thermo-Mechanical Reliability of TGV: Influence of Side wall angle and Copper Thickness	<114> Study on the Mechanism of Void-Free Nano-Through Silicon Via(TSV) Filling
	<683> Study on Delamination Mechanism of Semi-Insulating SiC Single Crystal Substrates During High-Temperature Vacuum Reflow: Electro-Thermo-Mechanical	<173> Electrografting of Ultralow-k Films on Si(111) via Sterically Hindered Diazonium Chemistry	<115> Robust SiC Package Reliability Study by Simulation	<762> Evolution of Interfacial Morphology and Joint Strength during Sintering of Nano-Ag Paste on (111)-Oriented Nanotwinned Cu Films
	<36> A Novel Mid-infrared Laser Debonding in Advanced Wafer-level Packaging	<348> Novel packaging epoxy resin with tunable thermal expansion coefficient and thermal conductivity designed for power devices	<140> Signal Integrity Characterization of Ultra-Fine Line RDL Interposer via Design, Simulation and Measurement	<164> Non-CMP Cu/SiO2 Hybrid Bonding Based on Interlocking Structure
	<725> Morphology and Wettability Evolution of Laser-Induced Carbon Residues during UV Laser Debonding	<357> Enhancing SR-Copper Interfacial Adhesion Under Wet-Thermal Conditions: A Facile Physical Blending Approach for Advanced Packaging Applications	<145> Prediction of Homogeneous Thermal and Mechanical Properties for PCB Conductive Layers Using an Attention-Based Deep Neural Network	<212> Metal micro-bump arrays printing via laser-induced metal microdroplets deposition
	/	<174> Advanced Adhesive Technology for Silicon Photonic and CPO Optical Packaging	<183> Design and Optimization of a TGV-Based V-Band Seventh-Order LTLR Interdigital Bandpass Filter	<228> Rapid Low-Temperature Sintering of Cu Microparticles with PEG via a Pre-Drying Process
15:10-15:50	Poster Session A			
Session	Room 1	Room 2	Room 3	Room 4
	Session 9	Session 10	Session 11	Session 12
	Hybrid Bonding Technology	Metallic Solder, Sintering, and Plating Processes	Thermal-Mechanical Modelling -I	Interconnection Technologies for High-Power Applications
Committee	Track 1-2-Advanced Packaging	Track 2-2-Packaging Materials & Processes	Track 3-2-Packaging Design & Modeling	Track 4-2-Interconnection Technologies
Chairs	Qian WANG, Tsinghua University Zhaohuan TANG, United Microelectronics Center	Zhuo LI, Fudan University Liang CAO, Anhui University	Hongbo QIN, Guilin University of Electronic Technology Fengman LIU, Institute of Microelectronics, Chinese Academy of Sciences	Wangyuan LI, Southwest Jiaotong University Pan LIU, Fudan University
15:50-16:15 Invited	Large-Field Projection Lithography: Technical Routes and Industrial Value of Full-Wafer Exposure for Advanced Packaging Dr. Bo-Fang PENG, PURECHIP, China	Technological Development and Applications of Ultra-Low Loss Fiberglass-Free Film Products in the Era of High-Performance AI Computing Dr. Yue JIANG, Guangdong EPS Technology Co., Ltd., China	Modeling and Simulation of Advanced Packaging with COMSOL Mr. Zhenhong ZHONG, COMSOL China	Structured Light for Subtle Micro- and Nanomachining of Transparent Materials and Beyond Dr. Daniel Flamm, TRUMPF SE + Co. KG, Germany
Oral	<437> In-situ XPS Analysis of Hydroxyl Group Generation in Plasma Activation Technology	<117> Research on Sintering Performance Optimization of Large-Area Cu Sintering for Press-Pack IGBT Packaging	<336> Thermal Modeling of Conductive Layers Using a Monoclinic Homogenization Method Considering Copper Wiring Orientation	<229> Study on Microstructure evolution and Properties for Direct Deposition of SAC305 Bumps by Pulsed Orifice Ejection Method
	<696> Low Temperature Cu-Cu Direct Bonding Enabled by PVD-Deposited CoxN Passivation Layer	<561> Superb sinterability of the Cu paste consisting of Cu micro-nano particles synthesized by a mild one-pot aqueous method for low-temperature in-air die	<380> Construction method of ultrasonic thermocompression bonding process model	<280> Polyimide-Based Low-Temperature Heterogeneous Bonding for Versatile Substrate Integration
	<410> Impact of Warpage on Misalignment and Voids in 5 μm Pitch D2W Hybrid Bonding	<43> Effect of Polyethylene Glycol Molecular Weight on the Die-Attach Performance of Pressureless Silver Sintering Paste	<521> Transient thermal-mechanical coupling simulation of IC product resistance soldering and its influence on the fatigue life of the wire bond during temperature	<312> Simulation and Design of Low-Reflection Vertical Interconnect for Differential High-Speed Serial Link in 2.5D Fan-Out Reconstituted Interposer
	<298> Effect of Surface Hydroxyl Density on SiO ₂ Bonding Behavior: A Molecular Dynamics Study	<641> Study on the Corrosion Behavior of Sintered Ag in Seawater	<533> Low-Stress Structure Optimization of Double-Sided Sintering for the Power Module by Taguchi-Grey Relational Analysis	<407> Development and characterization of ZnO-B2O3-SiO2 glass frit based silver paste for high-performance interconnects compatible to silicon nitride substrates
	<306> Revealing the Dynamics of Vortex-based Contactless Chip Pick-up via Fluid-Structure Coupled Analysis	<75> Investigation of Functional Additives for Cyanide-Free Au-Sn Alloy Electroplating and Its Application in Electronic Packaging	<542> Dominant Multiphysics Effects Governing In-Plane Distortion in Direct Wafer Bonding	<427> Enabling 5 μm Pitch D2W Hybrid Bonding: From CMP to Bonding Process Co-Optimization
	<213> Minimized intermetallic compound formation at Cu- Pillar bond interfaces through a dual-step laser- assisted reflow and laser-assisted bonding process	<205> Pressure Cu Sintering Paste Developed for Next Generation Interconnection Material	<543> Study on the Evolution Mechanism of Micro-Bump Contact Resistance in Chiplet Packaging Considering Electro-Thermo-Mechanical Coupling	<448> Fabrication of electroplated Sn-Cu foam for transient-liquid-phase bonding
	<589> A non-destructive metrology solution for prediction of bonding void and reliability in fusion and hybrid bonding	<741> Controlled One-Pot Synthesis of Copper Nanospheres through Aqueous Reduction for SiC Module Packaging	<581> Modeling and Optimization of TSV Cu Electroplating Process for Void-Free Filling	<450> NaOH-Based Wet Chemical Activation for SiCN Dielectric Bonding
	/	/	<474> Experimental and Numerical Investigation on Board-Level Drop Test Reliability of Fan-Out BGA Chip Considering PCB Assembly Process and Impact	<619> Research and Performance Investigation of Thermal Stress Mitigation Buffer Layers for TGV Metallization
18:30-21:00	Welcome Dinner			



August 6th PM Technical Sessions

Session	Room 5	Room 6	Room 7	Room 8
	Session 5	Session 6	Session 7	Session 8
	Characterization and Reliability	Reliability Testing and Modeling	Advanced Materials for Power Electronics	Optoelectronic Intergration
Committee	Track 5-1-Advanced Manufacturing	Track 6-1-Quality & Reliability	Track 7-1-Power Electronics & Energy Electronics	Track 8-Optoelectronics and New Display
Chairs	Zhiwen CHEN, Wuhan University Han JIANG, Anhui University	Yutai SU, Xi'an Xice Testing Technology Co., Ltd. Zhengwei FAN, National University of Defense Technology	Huaiyu YE, Southern University of Science and Technology Zhongmin XUE, Xi'an Jiaotong University	Haohui LONG, Shanghai Jiao Tong University Hanzhi MA, Zhejiang University
13:00-13:25 Invited	Opportunities and Challenges of FOPLP and Electroplating Technologies for Advanced AI Chip Packaging	End-to-End TGV AOI Metrology for Mass Production	Advanced Packaging Solutions and Thermo Mechanical Reliability Investigation for High Performance Embedded Power Modules	NPO/CPO Optical Engine Packaging in the AI Era: Discussions and Engineering Practices
	Mr. Zhaowei JIA, ACM Research (Shanghai), Inc., China	Mr. Yang YANG, Shenzhen Hanswell Technology Co., Ltd., China	Dr. Jing ZHANG, Heraeus Electronics China	Dr. Quan CAO, Wuhan Fisilink Microelectronics Technology Co., Ltd., China
Oral 13:25-15:10	<709> Impact of Source Lead Structure and Material on Electro-Thermal-Mechanical Performance and Electromigration Reliability of	<70> Electro-Thermo-Mechanical Analysis of CNTs-Cu-Filled TSV Arrays for Enhanced Reliability	<300> Minimizing TIM Thickness and Coolant Bypass in Double-Sided Cooled Automotive Power Modules via an Adaptive Split-Fin Architecture	<373> Design of a Field-Replaceable Hermetic VCSEL Optical Engine for High-Reliability CPO Interconnects
	<190> Electromigration-Induced Atomic and Stress Evolution in Copper Strips	<288> Multi-Physical-Field Coupled Life Prediction of PCB Assemblies Based on Contribution-Index-Calibrated Damage Accumulation	<16> Integration of superlattice-based thin-film thermoelectric module in β -Ga2O3 Schottky barrier diodes for simultaneous cooling and power generation	<184> Thermal Reliability of 80Au20Sn Solder Bump for Optoelectronic Heterogeneous Integration
	<326> Warpage Bifurcation Behavior of SiC and Si Interposer Wafers: A Thermo-Mechanical Analysis via RVE Modeling	<334> AI-based Prediction of Partitioned Equivalent Material Properties of Wiring Structure and Application to PCB Warpage Simulation	<112> Particle Morphology-dependent Microstructure and Fracture Toughness in Sintered Copper Particles	<488> Fabrication of a Quantum Dot Color Conversion Layer by Laser Patterning for Full-color Micro-LED Displays
	<705> Structural and Porosity Characterization of Acetic Acid-Modulated Mg-MOF-74 for Low-k Dielectric Applications	<532> A Physics-Guided Gradient Boosting Approach for Few-Shot Prediction of Plastic Work Density in BGA Solder Joints	<302> Investigation of high conductive Pressure-less copper sintering for SiC Power Package Bottleneck solution	<599> Advanced Cold-Sintered Phosphor Ceramics@Cu Converters toward Ultra-High-Brightness Laser Lighting
	<472> Characterization of Solder Interconnections Formed by Cu-Sn Nanocomposite Interlayers	<539> A Homogenized Equivalent Modeling Method for Multiphysics Simulation of 3D Stacked Chips	<639> From Silver to Copper: An All-Sintered-Cu Interconnection for SiC Power Modules	<759> Interfacial Delamination and Thermo-mechanical Reliability Analysis of an Embedded Pt-RTD Structure for in situ Wafer-Level Temperature Monitoring
	<317> Hybrid Qualification in Virtual Factory: A Data-Driven Framework for Cross-Site Manufacturing Consistency	<675> Computational Characterization of Interface Crack Initiation and Propagation in 16-Hi HBM4 with Hybrid Bonding TSV Structure under Thermo-	/	<Invited> Glass Substrates Enable Advanced Semiconductor Packaging: Design Rules for Via-Via Distances Based on Mechanic Reliability
	<469> Mechanism of Adhesive Residue Formation in Laser Debonding and Development of a Plasma-Assisted Cleaning Process for Temporary Bonding	<707> An In-depth Numerical Simulation Study on Interfacial Delamination and Cohesive Glass Fracture in Glass Substrate Packages with Multi- Layer RDLs		Dr. Martin Letz, SCHOTT AG, Germany
15:10-15:50 Poster Session A				
Session	Room 5	Room 6	Room 7	Room 8
	Session 13	Session 14	Session 15	Session 16
	Emerging Technologies for Advanced Packaging	Emerging Technologies for Flexible Electronics	3D Interconnect, Hybrid Bonding, and Integration Schemes	Thermo-Mechanical Simulation and Reliability Engineering
Committee	Track 10-1-Emerging Technologies	Track 10-2-Emerging Technologies	Track 2-3-Packaging Materials & Processes	Track 2-4-Packaging Materials & Processes
Chairs	Yanhong TIAN, Harbin Institute of Technology Daquan YU, Xiamen University	Zhi JIANG, Harbin Institute of Technology (Shenzhen) Su DING, Jiangnan University	Liyi LI, Dongnan University Liang ZHANG, Xiamen University of Technology	Caifu LI, Sun Yat-sen University Chuantong CHEN, Osaka University
15:50-16:15 Invited	AI is Accelerating the Shift to Advanced Packaging with PLP and Glass Cores	Electromigration in Microscale Interconnects with a Coexisting Liquid-Solid Solder Matrix	3D Heterogeneous Integrated DRAM for the Intelligent Era	From Solvent Engineering to Intelligent Design and Optimization: A Multiscale Study of Sintered Interconnect Materials
	Dr. Yik-Yee TAN, Yole Group, Singapore	Prof. Wu YUE, Lanzhou Institute of Technology, China	Dr. Fujun BAI, Company: Xi'an UniIC Semiconductors Co. Ltd	Dr. Pan LIU, Fudan University
Oral	<85> A Novel 3D Hermetic Stacked Packaging Structure Based on Kovar-Pillar Arrays for Spaceborne Electronics	<67> Electrospun stretchable BNNS/PVA composite film for efficient thermal management of flexible electronics	<261> Revealing the Effects of Particle Size and Distribution on the C2W Hybrid Bonding Dynamics	<482> Thermal Warpage Simulation of BGA Chip Considering Full Packaging Process and Underfill Property Test
	<121> Effects of Pre-drying on Microstructure and Shear Strength of Low-Pressure Sintered Micron-Ag Joints	<276> Self-Healing and Radiative-Cooling E-Skin for Advanced Thermal Management and Reliable Encapsulation	<179> Effects of Cu Film Microstructure on Bonding Performance of Cu-to-Cu Bonding: Interface Elimination Driven by Grain Growth Kinetics	<715> Warpage Study of Heterogeneous Integration in Die-first and Die-last FOWLP
	<278> Indium-capped Copper Pillar Flip-chip Scheme Compatible for 2.5D Superconducting Quantum Computing Architecture	<327> Self-powered flexible humidity sensor based on graphene oxide films constructed by metal reduction	<676> Fabrication and Key Process Optimization of 2.5D CoWoS High Density MCM with HBM Integration	<481> Challenges during the development of Epoxy Mold Compounds (EMC) in high voltage devices for automotive applications
	<406> A Universal Monolithic Integration Strategy for Perovskite Single Crystals via Ionic-Liquid-Mediated Chemical Welding	<344> An Experimental Study on Non-Invasive Flexible Electronic Sensing Technology for Mimosa Pudica Action Potential Detection	<194> Discovery of High-Performance Low-k Interconnect Materials via Multi-Target Machine Learning Model	<582> Synergistic Design-Process-Material Optimization for Suppressing Solder Ball Voids in Embedded Silicon Fan-Out (eSiFO) Packaging
	<478> Preliminary Study of Photoresist Thermal Reflow for Silicon Bridge Positioning	<465> Three-Dimensional Crosslinked PEG-Based Composite Phase Change Material for Enhanced Thermal Management in Electronic Packaging	<374> Reversible Adhesion Electromagnetic Shielding Film for PCBA Board-Level EMI Conformal Shielding Packaging	<31> Corner Wire Sweep Improvement for HDQFP Package
	<627> Process Development and Suppression of Stress and Warpage in embedded Glass Fan-Out Packaging	<564> Semi-Sintered Copper Pastes with High Conductivity and Strong Adhesion for Printed Electronics	<91> Design of a 3D Compact Bandpass Filter Based on Dual-Layer Interconnect Structure	<201> Balancing Mechanical Support and Thermal Stress Management in Underfill for Advanced Electronic Packaging
	<760> Tuning Twin Formation in β -Sn: Effects of Indium and Cooling Rate in SAC305-xIn Solder Balls	<701> Application of Electrostatic Printing Technology in Embodied Intelligence-Oriented Flexible Sensors	<71> Synergistic Additive Formulation and Electrochemical Analysis for Copper Grain Refinement in Advanced Semiconductor Packaging	<65> Comparative Study on High-Temperature Aging Behavior of SIBAC and SAC305 Solders
18:30-21:00	/	/	<286> A Study on Optimization of Mold-flow Balance for SIP Packages	/
	Welcome Dinner			



August 7th AM --- Technical Sessions

Session	Room 1	Room 2	Room 3	Room 4
	Session 17	Session 18	Session 19	Session 20
	Co-Packaged Optics at Scale	ICEPT-ICEP Joint Session	Co-packaging of Optoelectronics and Thermal Management	Thermal-Mechanical Modelling -2
Committee	/	/	Track 1-3-Advanced Packaging	Track 3-3-Packaging Design & Modeling
Chairs	Farhang Yazdani, BroadPak Corp. Qidong WANG, IMECAS	Yasuhiro Morikawa, ULVAC, Inc. Junsha WANG, Meisei University	Shenglin MA, Xiamen University Chi ZHANG, Peking University	Jun WANG, Fudan University Hongbin SHI, Awinic Technology Co., Ltd.
8:30-8:55 Invited	<8:30-8:45> Intelligent manufacturing solutions for advanced CPO, LPO, NPO & OCS Mr. Alex CAO, ficonTEC China <Invited> Photonic Packaging Dr. Yik-Yee TAN, Yole Group, Singapore <Invited> Advanced Organic Substrates Enabling Co-package Optics at Scale Mr. Bula WANG, AT&S, China Panel Discussion	Cu Paste for Bonding Applications in Advanced and Power Semiconductor Devices Prof. Chuantong CHEN, Osaka University, Japan <Invited> Thin Film Applications via Atomic Layer Deposition (ALD) in Advanced Packaging Processes Mr. Zihao LI, Kokusai Electric Corporation, Japan <Invited> Composite Materials for Effective Heat Dissipation Application Mr. Bin XU, University of Tokyo, Japan <Invited> Advanced Wafer Temporary Bonding and Debonding Tape Solutions for 3D Packaging Mr. Weiqiang SHEN, Sekisui (Shanghai) International Trading Co.,Ltd., China	From Round to Rectangle: NAURA Empowers the Development of Panel-Level Packaging Mr. Yang WANG, Beijing NAURA Vacuum Technology Co., Ltd., China <206> Warpage Optimization for Near-Packaged Optics (NPO) in 3.2T Optical Modules for AI Computing Center Network Interconnects <291> Thermal Conductivity Characterization of Nano-Interconnects for Hot Spot Mitigation in Advanced Packaging <303> Targeted Cooling of Local Hotspot with Prenucleation-Assisted Ice-Templating Method <Invited> Process challenges and failure analysis of semiconductor packaging substrates and high-density interconnects Ms. Wenjing WEI, AT & S	Mastering 3D-IC Design Challenges Through Advanced Simulation Mr. Minggang HOU, Synopsys, USA <617> Study on Heat Transfer and Phase Change Features of Metal Foam-Enhanced Phase Change Composites <673> Temperature-Dependent Interfacial Thermal Resistance of GaN/AlN Heterostructures: Role of Ga/N Vacancy in the Near-Interface Region <680> Coupled thermo-mechanical analysis and reliability-oriented optimization of cylindrical pin-fin embedded microchannels for 3D-ICs <730> Design and Analysis of a Flip-Chip SiP T/R Module with High Heat Dissipation Performance <318> Warpage Simulation of Molded Wafer with Silicon Bridges and TMVs
10:10-10:50	Poster Session B			
Session	Room 1	Room 2	Room 3	Room 4
	Session 25	Session 26	Session 27	Session 28
	Co-Packaged Optics at Scale	Design and Applications of Power Device and module	Ceramic Substrates and Thermal Conductivity Enhancers	Packaging Optimization Modelling
Committee	/	Track 7-2-Power Electronics & Energy Electronics	Track 2-5-Packaging Materials & Processes	Track 3-4-Packaging Design & Modeling
Chairs	Farhang Yazdani, BroadPak Corp. Qidong WANG, IMECAS	Zhaozheng HOU, Huawei Digital Power Technologies Co., Ltd. Fengtao YANG, Xi'an Jiaotong University	Zhiqian LIU, Southern University of Science and Technology Li LIU, Delft of Technology	Pei CHEN, Beijing University of Technology Meiyang SU, Institute of Microelectronics of the Chinese Academy of Sciences
10:50-11:15 Invited	<10:50-11:05> Material Technologies Enabling Co-Packaged Optics: Challenges and Solutions in Electronic-Photonic Hybrid Integration Dr. Yasuharu Murakami, Resonac Corporation, Japan	Research on 10Gbps Space Balanced Photodetector Based on Metallized Fiber Resistance Welding Technology Ms. Zhen MA, Academy of Space Electronic Information Technology, Xi'an Branch, China	Process and Material Challenges and Solutions for Ultra-large-scale Chiplet Advanced Packaging Dr. Hongbin SHI, Awinic Technology Co., Ltd., China	Advanced Utilisation of Machine Learning Models for Package Reliability Analysis Dr. Karsten Meier, Technische Universität Dresden, Germany
11:15-12:30 Oral	<Invited> Innovative Materials for Next-Gen Package Substrates and Co-Packaged Optics (CPO) Mr. Habib Hichri, Ajinomoto Fine Techno Corporation, USA <Invited> Breaking the Laser Bottleneck: Simplifying Co-Packaged Optics Manufacturing with 60x Fewer DFB Lasers Mr. Pirooz Hojabri, IC Photonics Panel Discussion	<125> Reliability Assessment and Multi-Stress Lifetime Modeling of 1200 V SiC MOSFETs for Low-Voltage Power Distribution <13> A Unified Single-Phase Equivalent Circuit for Multi-Phase Buck Converters Considering Phase-Overlap Effect <50> Multi-Functional Low-Voltage Inverter Integrated System-in-Package for Joint Module Controller <330> An Active Temperature Control System Based on Thermoelectric Cooling for Improving the Thermal Management Stability of Power Modules <523> Power electronics chip rework without thermal and mechanical process	<329> Anisotropic constituents co-reinforced AlN fiber-based composite substrate with high flexural strength and thermal conductivity <491> Quasi-Hermetic Sealing Technology for Three-Dimensional Ceramic Substrates Using Adhesive Bonding <351> Microstructure and Properties of Carbon/Cu Composites for Thermal Management Applications <742> Design of Poly(ionic liquid)/Silver-Liquid Metal Composites for High-Performance Thermal Interface Materials /	<343> Effect of Surface Topography on Interfacial Reliability in Al Wire Bonding of SiC Power Chips <393> A Low-Parasitic-Inductance Double-Sided Cooling Silicon Carbide Power Module Featuring 3D Mutual Inductance Cancellation <444> Thermo-Mechanically Coupled TPF-CZM for Crack Evolution Analysis in IMC Layer Structures <335> Fatigue Life of Sn37Pb under Coupled Electro-Thermal-Mechanical Loading <471> Reliability-Oriented Design Optimization for Low Cost Panel-Level Packages (PLP)
12:30-13:30	Lunch			



August 7th AM --- Technical Sessions				
Session	Room 5	Room 6	Room 7	Room 8
	Session 21	Session 22	Session 23	Session 24
Committee	AI for Packaging Thermal Management	Process and Design Optimization	RF Packaging	Manufacturing Process and Interconnection
	Track 11-1-AI-Enabled Packaging Technologies	Track 6-2-Quality & Reliability	Track 9-RF Electronic Packaging	Track 5-2-Advanced Manufacturing
Chairs	Hongbin SUN, Xi'an Jiaotong University Cheng WANG, Shanghai Jiaotong University	Xiaofeng YANG, China CEPREI Laboratory Kui LI, Beijing Institute of Aerospace Microsystems and Information Technology	Nan WANG, Shanghai University Bo SUN, Guangdong University of Technology	Zili ZHANG, Institute of Microelectronics of the Chinese Academy of Sciences Shuibao LIANG, Hefei University of Technology
8:30-8:55 Invited	Transient Radiation Effects on Packaged Micro-systems	Failure Mechanism and Reliability Evaluation of Interconnection Structures for SiP	Q-band 4×4 Phased-Array Antenna-in-Package (AiP) for High-Efficiency mmWave NTN Applications	Advanced Die Attachment Technologies for Power Electronic Packaging
	Prof. Guohe ZHANG, Xi'an Jiaotong University, China	Dr. Ling LI, Xi'an Microelectronics Technology Institute, China	Dr. Li-Cheng SHEN, Universal Global Scientific Industrial Co., Ltd., Taiwan, China	Dr. Li LIU, Delft of Technology
8:55-10:10 Oral	<34> A Digital Optimization Framework for Thermal and Mechanical Performance of SiC Power Module Packaging	<93> Investigation of Set Design Parameters on Package Crack Failure Mechanisms in Set-Level Drop Test	<10> A High-Integration D-Band Terahertz Radiator Enabled by 3D Metal Micro-Coaxial Technology and SiP Integration	<126> Study on Hybrid Force/Position Control Considering Thermal Disturbances in Chip Thermo- Compression Bonding
	<98> FNOPlace: Fourier Neural Operator-Accelerated Thermally Aware Chiplet Placement for 2.5D Packaging	<102> Investigation and improvement of Delamination Failure in LQFP 10×10 Dual-Die Package	<325> AI-Assisted Robust Design of Ku-Band Dual-Polarized AiP Antennas Considering Manufacturing Tolerance	<494> A Copper Foil-Based Imprinting Method for Fabricating Embedded Lines with Enhanced Reliability
	<435> Physics-Informed POD-Guided Deep Learning Framework for Sparse Thermal Field Reconstruction	<221> Study on mechanism and improvement of Nanovoid in Blind Via for Advanced Packaging Substrates	<744> An Evanescent-Mode Rectangular Waveguide Bandpass Filter Using Post Arrays	<479> Enhanced Low-Temperature Cu–Cu Bonding with Mixed-Size Cu Nanowire Arrays
	<515> Efficient Thermal-Aware Chiplet Placement of 2.5D Heterogeneous Systems Using an Improved Multi-Fidelity Bayesian Optimization Framework	<245> Effect of Underfill Properties on Flip-Chip Reliability in No-Clean Processes	<731> Wafer-Level Thin-Film Packaging for 2.4 GHz Film Bulk Acoustic Resonator Filters	<90> Rapid and Scalable Fabrication of Coaxial 3D-Printed Interconnects for Multiplexed Microfluidic Systems
	<686> Rapid Prediction of Orthotropic Coefficients of Thermal Expansion for 2.5D Chiplet Packaging RDL	<588> Investigation of Crack Formation Mechanism in PECVD Silicon Dioxide Gap Filling in Chiplet Integration	<626> 3D On-chip Integrated Capacitors with Self-inductance Cancellation for Wideband RF Application	<733> Simulation Study and Experimental Validation for Optimization of Gas Distribution Plate Structure and Improvement of Plasma Photoresist Stripping in Fan-out Panel-level Packaging (FOPLP)
10:10-10:50	Poster Session B			
Session	Room 5	Room 6	Room 7	Room 8
	Session 29	Session 30	Session 31	Session 32
Committee	Deep Learning based Packaging Process	Failure Analysis	Testing and Characterization	Advanced Bonding Technologies
	Track 11-2-AI-Enabled Packaging Technologies	Track 6-3-Quality & Reliability	Track 4-3-Quality & Reliability	Track 4-3-Interconnection Technologies
Chairs	Yang HU, Tsinghua University Shizhao WANG, Hainan University	Yanwei DAI, Beijing University of Technology Yi ZHONG, Xiamen University	Sha XU, Guangdong University of Technology Bin ZHANG, Xi'an Jiaotong University	Yunwen WU, Shanghai Jiao Tong University Zhuo CHEN, Central South University
10:50-11:15 Invited	Biocompatible Ultrathin Devices Interfacing with Organs	Applications and Practices of Ultrasonic Imaging Technology in Quality Control	Experiment and Simulation on Mechanical Properties for Electronic Packaging Reliability	
	Prof. Zhi JIANG, Harbin Institute of Technology (Shenzhen), China	Dr. Gujin Hu, Shaoxing Xinjiyuan Electronic Technology Co., Ltd., China	Dr. Chuantao HOU, Beijing Institute of Structure and Environment Engineering, China	Yue SUN
11:15-12:30 Oral	<170> D ² -DINO: Difference-Aware Feature Pyramid Networks and Defect Token Priors for High Precision PCB Defect Detection	<158> Mechanism of electron irradiation induced dissolution of the Ag3Sn in SAC305	<74> A new method to test the value of Rjc-bottom for a BGA chip with T3ster	<490> Fabrication of a Multifunctional Adhesion Layer for Glass Substrate Electroplating
	<411> Machine Learning-Assisted Numerical Investigation on Multiphysics Coupling for Copper Electroplating in High Aspect Ratio Through Glass Vias	<175> Microstructural evolution and interfacial stability of a novel low-temperature Sn14In3Ag1Zn/Cu solder joints under isothermal aging	<99> Study of Keep-Out Zone (KOZ) Characteristics for Parylene-Liner TSVs Fabricated by Double-Sided Processes	<500> Pressureless Sintering of Ag Paste on Cu Interface in N2 Atmosphere Assisted by Silver Acetate
	<301> Knowledge-Informed Ensemble Learning for Dual-Interface Intermetallic Compound Thickness Prediction in Ball Grid Array Reflow Soldering	<319> Electromigration investigation of Sn40Pb C4 Bumps under High-Temperature and High-Current-Density	<536> Mechanical Properties and Interfacial Reaction Behavior of SACZAT/Cu Solder Joints	<547> Influence of Interfacial Energetics on Void Morphology and Closure in Cu-Cu Bonding
	<592> A Physics-Informed Conditional Diffusion Model for Prediction of Abrasive Particle Trajectories and Distribution in CMP Process	<390> Corrosion Behavior of Cu Pads and Cu/Ti Interfaces in Post-CMP Cleaning for Hybrid Bonding	<586> Broadband Electrical Analysis of Hybrid Bonding Interface Non-Idealities in 3D RDL-TSV Interconnects	<712> Atomic-Scale Investigation of Interfacial Healing Mechanisms in Indium-Indium Bonding
	<637> A Feature-Driven Approach for Chip Floorplan Inference Based on Dynamic Thermal Maps	<647> Interfacial Evolution and Electromigration Behavior of Cu–Ni–Cu–Sn Microbumps for Long-term Power Delivery in 3D IC Advanced Packaging	<507> High-Throughput Thermodynamic Screening of Multicomponent Solders for Reliable Interconnections in Advanced Packaging	<758> PE340 Silver Sinter Die Attach Paste: Tailored Rheology for High-Precision Stencil Printing and Dispensing
12:30-13:30	Lunch			



August 7 th PM --- Plenary Talk	
<i>Chair</i>	<i>Johan LIU, Academician of the Royal Swedish Academy of Engineering Sciences, Sweden</i>
13:30-14:00	Holistic Chiplet Packaging Approach
	<i>Dr. Tanja Braun, Head of Department, Fraunhofer IZM</i>
14:00-14:30	Advanced Packaging Materials Innovation through Co-creative Activities
	<i>Hidenori ABE, CTO for semiconductor materials, Executive director, Electronics Business Headquarters, Resonac Corporation, Japan</i>
14:30-15:00	Advanced Packaging Equipment Empowers a New Ecosystem of Heterogeneous Integration
	<i>Mr. Fei Yu, Beijing NAURA Microelectronics Equipment Co.,Ltd., China</i>
15:00-15:30	Application of Wafer Bonding in Advanced Packaging
	<i>Mr. Weijia CAI, CTO of Wushi Microelectronics (Suzhou) Co., Ltd, China</i>
15:30-16:10	Poster Session C
<i>Chair</i>	<i>Prof. Zhiquan LIU, Southern University of Science and Technology, China</i>
16:10-16:40	Getting ready for the challenges of Silicon Photonics
	<i>Ruby YAN, Vice president for global business center, Guangzhou Zen Semiconductor Corporation, China</i>
16:40-17:10	Chips Z: 2.5D/3D AI EDA+ Ushering in a New Era of STCO-Driven System-Level Collaboration for Advanced Packaging
	<i>Dr. Alex Zhao, Zhuhai Silicon Chip Technology Ltd., China</i>
17:10-17:40	Semiconductor Industry – Impact of Wafer Fabrication Equipment and Its Respective Processes and Critical Materials for Advanced Packaging
	<i>Dr. Kitty Pearsall, Kitty Pearsall, IEEE Fellow, EPS Distinguished Lecturer, EPS Past President</i>
17:40-18:10	Navigating the Collision of AI, Politics & Engineering Reshaping Electronics Manufacturing!
	<i>Dr. Charles Bauer, TechLead Corporation</i>
18:30-20:00	Closing Dinner (Invited Only)



OVERVIEW OF POSTER PRESENTATION SESSIONS

Poster Session A															
Thursday, August 6 th , 2026, 15:10-15:50															
Area1		Area2		Area3		Area4		Area5		Area6		Area7		Area8	
Track 1 Advanced Packaging		Track 2 Packaging Materials & Processes		Track 2 Packaging Materials & Processes		Track 3 Packaging Design & Modeling		Track 4 Interconnection Technologies		Track 3 Packaging Design & Modeling		Track 6 Quality & Reliability		Track 1 Advanced Packaging	
Track 7 Power Electronics & Energy Electronics		Track 11 AI-Enabled Packaging Technologies		Track 10 Emerging Technologies		Track 5 Advanced Manufacturing		Track 8 Optoelectronics and New Display		Track 9 RF Electronic Packaging				Track 6 Quality & Reliability	
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Poster Session B															
Friday, August 7 th , 2026, 10:10-10:50															
Track 1 Advanced Packaging		Track 2 Packaging Materials & Processes		Track 2 Packaging Materials & Processes		Track 3 Packaging Design & Modeling		Track 4 Interconnection Technologies		Track 3 Packaging Design & Modeling		Track 6 Quality & Reliability		Track 1 Advanced Packaging	
Track 7 Power Electronics & Energy Electronics		Track 11 AI-Enabled Packaging Technologies		Track 10 Emerging Technologies		Track 5 Advanced Manufacturing		Track 8 Optoelectronics and New Display		Track 9 RF Electronic Packaging				Track 6 Quality & Reliability	
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Poster Session C															
Friday, August 7 th , 2026, 15:30-16:10															
Track 1 Advanced Packaging		Track 2 Packaging Materials & Processes		Track 2 Packaging Materials & Processes		Track 3 Packaging Design & Modeling		Track 4 Interconnection Technologies		Track 3 Packaging Design & Modeling		Track 6 Quality & Reliability		Track 1 Advanced Packaging	
Track 7 Power Electronics & Energy Electronics		Track 11 AI-Enabled Packaging Technologies		Track 10 Emerging Technologies		Track 5 Advanced Manufacturing				Track 9 RF Electronic Packaging				Track 6 Quality & Reliability	
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