OVERVIEW OF PROFESSIONAL DEVELOPMENT COURSE

Wednesday, August 5th, 2026, 08:30-21:30

Room 1 - Room 4

Time	Room 1	Room 2	Room 3	Room 4
08:30-10:10	**PDC 1 - Driving the Megawatt AI Era: Next-Gen Packaging** *Scott CHEN* *ASE Group*	**PDC 3 - Advanced System Packaging and Solder Interconnection** *Way Koh, Jusheng MA* *Pacrim Technology, Tsinghua University*	**PDC 5 - Cu-Cu Hybrid Bonding and Co-Packaged Optics with Silicon Photonics** *John LAU* *Unimicron Technology Corporation*	**PDC 7 - Photonic Components and Packaging Technologies for Optical Links** *Torsten Wipiejewski* *Huawei Technologies Duesseldorf GmbH*
10:10-10:25	*Break*			
10:25-12:05	**PDC 2 - Nano Materials and Polymer Composites for Electronic Packaging** *Zhuo LI* *Fudan University*	**PDC 4 - High Reliability Soldering in Semiconductor Packaging** *Ningcheng LI* *IEEE Fellow*	**PDC 6 - Wafer Bonding and Hybrid Bonding Technologies: From Fundamentals to Frontier Applications** *Chenxi WANG* *Harbin Institute of Technology*	**PDC 8 - Experimental Methods for Stress and Strain Analysis of Advanced Electronics Packaging** *Jeff Suhling* *Auburn University*
12:05-13:00	*Break*			

Mr. Scott CHEN

Senior Vice President of Engineering, ASE (Advanced Semiconductor Engineering), Taiwan, China

Topic: Driving the megawatt AI Era: Next-Gen packaging
Biography: Mr. Scott Chen received B.S. degree in Chemical Engineering from NTU (National Taiwan University). And master's degree of Executive MBA Program from NTU. He has been worked on each of assy technology, MEMS nsor, bumping, flip chip, advance package technology and SIP solution over 30 yrs.

Prof. Zhou Li

Professor, Fudan University

Topic: Nano Materials and Polymer Composites for Electronic Packaging
Biography: Prof. Zhuo Li is a Professor in the College of Smart Materials and Future Energy, and a PI in the State Key Laboratory of Molecular Engineering of Polymers at Fudan University, where her research focuses on functional polymer composites for flexible sensors and electronic packaging. She earned her B.S. degree from Tongji University, followed by an M.S. from Virginia Tech and a Ph.D. from the Georgia Institute of Technology. Before joining Fudan, Dr. Li worked as a Materials Engineer at Celanese Corp. and CNPC USA Corp. She has published over 90 papers in journals such as Science Translational Medicine, Nature Communications, Advanced Materials. Currently, she serves as an Associate Editor for IEEE TCPMT, Chair of the IEEE-EPS Shanghai Chapter, Chair of the IEEE-WIE Shanghai Affinity Group, and a member of the ICEPT Packaging Materials and Processes Committee. Dr. Li was a recipient of the IEEE EPS Outstanding Young Engineer Award in 2020.

Abstract: Nano materials and polymer composites are widely used in electronic devices as adhesives, encapsulants, thermal interface materials, insulators, dielectrics, conducting elements for interconnects. This short course will provide overview on the latest advancement of nano materials and composites, and their impact to advanced electronics packaging and integration.

Prof. Jusheng MA

Professor, Tsinghua University

Topic: Low-Temperature Solder Interconnection for Packaging

Abstract: This lecture will examine the property optimization and performance enhancement of SnZn- based low- temperature solders, their behavior during reflow assembly, solder- joint reliability and failure mechanisms, and the advantages these alloys offer for modern high- performance packaging—along with future development prospects.

SnZn- based low- temperature lead- free solders were developed to match the service characteristics of SnPb37 while providing an environmentally friendly alternative to SnAg3Cu0.5. Their key attributes include:

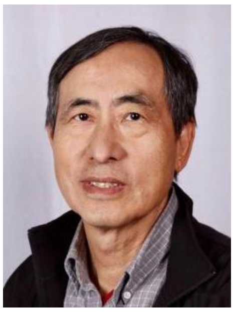
• Thermal properties comparable to SnPb37, enabling seamless use with existing equipment and low- temperature devices originally designed for SnPb37 processes.

• Substantially improved solder- joint reliability relative to SnPb37, including enhanced thermal- fatigue resistance, oxidation resistance, and mechanical strength.

• Wettability superior to SnAg3Cu0.5 and on par with SnPb37, supporting robust joint formation across a wide range of metallizations.

• Higher joint strength and environmental reliability than SnAg3Cu0.5, making them suitable for advanced and reliability- sensitive applications.

The discussion will also highlight the economic and manufacturing benefits of SnZn- based alloys, such as reduced SMT reflow temperatures, lower power consumption, decreased material cost, improved reliability, and reduced thermal stress to high- performance and large- form- factor packages.



Dr. Wei Koh

Founder, Pacrim Technology Irvine, CA, USA

Topic: System Level Packaging Integration

Biography: Dr. Wei Koh has worked in the IC packaging and microelectronics assembly technologies for 40 years at Henkel, Motorola, and others. He is an IEEE Fellow with over 100 publications and 40 patents. He received his PhD from Cornell University.

Abstract: Modern IC packaging for AI/HPC is rapidly evolving, with heterogeneous chiplet integration expanding beyond traditional System- in- Package (SiP) architectures toward large- format system- level integration modules—some reaching sizes of up to 125 mm × 125 mm.

This course will review several state- of- the- art large system- level integrated modules, including Nvidia's CoWoP platforms, AMD's SiP packaging progress, and Intel's Panther Lake CPU module. The discussion will then examine the key integration components and enabling technologies, such as 2.5D silicon interposers, embedded bridging, and 3D TSV- based HBM stacks, along with FOPLP glass panel processing. The course concludes with an overview of emerging technology trends and the major challenges facing next- generation system- level module integration for AI/HPC.

Dr. Ning-Cheng LEE

Founder, ShinePure Hi-Tech, China

Topic: High Reliability Soldering in Semiconductor Packaging

Biography: Dr. Ning-Cheng Lee is founder of ShinePure Hi-Tech. Prior to that, he was the Vice President of Technology of Indium Corporation. He has been with Indium from 1986 to 2021. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 30 years of experience in the development of fluxes and solder materials for SMT industries. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies" by Newnes, and co-author of 5 other books. He received 1991 award from SMT Magazine and 1993 and 2001 awards for best proceedings papers of SMI or SMTA International Conferences, 2003 Lead Free Co-Operation Award from Soldertec, 2008 and 2014 awards from IPC for Honorable Mention Paper – USA Award of APEX conference, and 2010 Best Paper Award of SMTA China South Conference. He was honored as 2002 Member of Distinction from SMTA, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, 2010 Electronics Manufacturing Technology Award from CPMT, 2015 Founder's Award from SMTA, and 2017 IEEE Fellow.

Abstract: Semiconductor soldering is much more delicate and is very critical for reliability of devices. This course covers the critical parameters governing the reliability for soldering in semiconductor packaging. The reliability discussed includes parameters affecting the intermetallic compounds (IMC), voiding, electromigration, low temperature soldering, high temperature soldering, and electrochemical migration under a variety of material combinations. The failure modes are discussed in details, with preferred choices of materials and designs recommended.

Course Content:

• IMC

• Voiding–Effect of Cu Pad Grain Size on IMC–Interaction of Cu and Ni–Effect of Base Metal Co-P on IMC–Effect of Solder Form on Voiding–Effect of Joint Height, Temperature, Electrical, Mechanical on Shear Strength, IMC, Kirkendall Voiding–Effect of Cu Structure on Kirkendall Voids

• Electrochemical Migration (ECM)

• EM

• LTS–Effect of EM vs TC on Crack Formation –Effect of Back Stress on EM–Effect of Grain Orientation on EM–Effect of RDL Design on EM–Electromigration of Low Temperature Sn-57Bi-1Ag–Electromigration of LTS - Alloy Effect –Electromigration of LTS - Surface Finish Effect –Bi-Rich Whisker Growth–TCT Reliability of LTS –Collapse of LTS –Deposition, Hot Tear, Bi Stratification of LTS –Hot Tear of Homogeneous LTS BiSn- Effect of Profile & Surface Finish–Drop Test of LTS

• HTS - TLPB (Transient Liquid Phase Bonding)

Dr. John H Lau

Chief Scientist, Unimicron Technology Corporation, Taiwan, China

Topic: Cu-Cu Hybrid Bonding and Co-Packaged Optics with Silicon Photonics

Biography: Dr. John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 535 peer-reviewed papers (385 are the principal investigator), 52 issued and pending US patents (31 are the principal inventor), and 24 textbooks. John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

Abstract: Cu-Cu hybrid bonding is one of the flip-chip bumpless assembly technologies. The advantages of hybrid bonding are: (a) higher density, (b) finer pad pitch, and (c) better electrical and thermal performance. In this lecture, 21 high-volume manufacturing (HVM) or to be HVM products and 12 new applications using hybrid bonding will be presented. On the other hand, co-packaged optics (CPO) are heterogeneous integration packaging methods to integrate the chiplets in switch, photonic ICs (PIC) such as lasers and photodiodes, and electronic ICs (EIC) such as the laser driver and the transimpedance amplifier (TIA). The advantages of CPO are: (a) to reduce the length of the electrical interface between the PIC/EIC and the switch, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance. In the next few years, we will see more implementations of Cu-Cu hybrid bonding and a higher level of heterogeneous integration of switch, EIC and PIC with silicon photonic, whether it is for performance, form factor, bandwidth, power consumption or cost. The content of this lecture is shown below.

- Introduction
- Origin of Hybrid Bonding
- Fundamentals of Cu-Cu Hybrid Bonding
- 21 HVM Products with Cu-Cu Hybrid Bonding
- 12 New Applications for Cu-Cu Hybrid Bonding
- Data Centers, Switch, EIC, and PIC
- OBO (on-board optics), NPO (near-board optics), CPO (co-packaged optics)
- 3D Heterogeneous Integration of Switch, PIC and EIC with Bridges and/or Glass Substrate/Interposer
- CPO with Silicon Photonics: Silicon Waveguides, Coupler, etc.
- Summary and Recommendations

Dr. Chenxi WANG

Professor, Harbin Institute of Technology

Topic: Wafer Bonding and Hybrid Bonding Technologies: From Fundamentals to Frontier Applications

Biography: Dr. Chenxi Wang is a full professor at Harbin Institute of Technology (HIT), a recipient of the National First-Class Course Award (China), and received Ph.D. from The University of Tokyo. His research interests include wafer bonding, heterogenous/hybrid chip bonding, 3D integration and packaging, and joining of medical materials. He was a Research Fellow of the Japan Society for the Promotion of Science (JSPS) and participated in the JST-CREST (Core Research for Evolutionary Science and Technology). After returning to China, he has led four projects supported by the National Natural Science Foundation of China (NSFC), and undertaken over 20 provincial and industrial research projects. He has published more than 140 SCI/EI papers and received seven Best Paper Awards from international conferences. He holds 17 authorized invention patents. He serves as a technical committee member of ICEPT (International Conference on Electronic Packaging Technology), a senior member of IEEE, and a senior member of the Chinese Mechanical Engineering Society (CMES). His honors include the Chinese Government Award for Outstanding Self-Financed Students Abroad, the Dean's Award from the School of Engineering, the University of Tokyo, and the First Prize of Natural Science Award of Heilongjiang Province. In teaching, he has won multiple first prizes in provincial and university-level teaching competitions. He was the supervising instructor of the champion team (Grand Prize, first place) in the “Challenge Cup” National College Student Extracurricular Academic and Technological Works Competition. He has led four educational reform projects and co-authored two textbooks.

Abstract: In recent years, wafer direct bonding technology, which requires no intermediate layers, has gained significant attention and is widely used in areas such as single-crystal thin-film composite substrates, MEMS packaging, and heterogeneous integration. Conventional silicon fusion bonding, requiring excessively high temperatures, tends to cause thermal diffusion and thermal stress issues between dissimilar wafers, making it difficult to meet the diverse and high-density integration demands of the post-Moore era. Therefore, developing low-temperature or even room-temperature bonding technologies for heterogeneous materials has become an inevitable trend. This course introduces the fundamental principles and evolution of wafer bonding, with a focus on the technological development and core differences between ultra-high vacuum surface activated bonding (SAB) and plasma activated bonding (PAB). In addition, the course provides a discussion on the bumpless hybrid bonding technology for 3D integration, covering key challenges such as high-precision Cu/SiO2 alignment, interface defect control, and low-temperature processing. Covering the innovation path from conventional wafer bonding to advanced hybrid bonding, this course explores strategies to overcome thermal budget limitations, offering technical support for future high-performance heterogeneous integration.

Dr. Torsten Wipiejewski

Director, Huawei Technologies Duesseldorf GmbH

Topic: Photonic Components and Packaging Technologies for Optical Link

Biography: Dr. Torsten Wipiejewski joined Huawei Technologies in 2014 and is responsible for the European technology sourcing of Huawei's Hardware Engineering Institute. His interest covers all hardware aspects for products ranging from smart watches to optical communication systems. He has also been appointed as Technical Advisor to the President of Huawei's European Research Institute. Previously, Torsten was an investor in renewable energy, CEO at Optogan (Germany, Finland) making blue LEDs, and COO at Firecomms (Ireland) making optical transceivers for automotive applications. He also held management positions at ASTRI in Hong Kong, Agility Communications in Santa Barbara, CA, USA as well as Infineon, Osram, and Siemens in Germany. Torsten received a "summa cum laude" Ph.D. degree in electrical engineering from the University of Ulm, Germany and has been an executive member of several international conferences. He was the General Chair of ECTC 2008 and has lectured several courses at conferences and universities. He holds more than 30 patents and has published over 100 scientific papers and presentations.

Abstract: This course will provide an overview on the various photonic components and packaging technologies that enable optical interconnects. These applications are key for the information and communication technology of today and path a way to the future. High speed optical interconnects from board level in data centers to long haul transmission systems requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of various types including VCSELs, high speed optical modulators and photodetectors.

AI has become a major driver to increase data throughput in data centers and high-performance computing. Optical interconnects offer a large bandwidth and can help to reduce energy consumption for data transfer. Bringing the optical engine close to the GPU/ASIC core is the target of co-packaged optics (CPO) solutions replacing the electrical signal lines on board level. Packaging technologies play a key role in the implementation of optical solutions, because the cost of the system is typically dominated by the assembly and packaging cost. Integration schemes such as photonic integrated circuits (PICs) have become mainstream technologies for cost and size reduction. We will discuss optical waveguides and the coupling of optical waveguides and components to optical fibers. This is a key challenge in optical packaging because of the tight alignment tolerances.

Prof. Jeffrey Suhling

Quina Professor and Department Chair, Department of Mechanical Engineering, and Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3), Auburn University, USA

Topic: Experimental Methods for Stress and Strain Analysis of Advanced Electronics Packaging

Biography: Prof. Jeffrey Suhling received his Ph.D. degree in Engineering Mechanics from the University of Wisconsin in 1985. He then joined the faculty of the Department of Mechanical Engineering at Auburn University, and currently holds the rank of Quina Distinguished Professor. He served as the Center Director for the NSF Center for Advanced Vehicle Electronics (CAVE) from 2002-2008, and as ME Department Chair from 2008-2025. His research concentrates on the mechanics, reliability, and materials science of electronic packaging and semiconductors; with emphasis on stress sensors and test chips, material characterization and constitutive modeling, and reliability testing and modeling. Dr. Suhling has co-authored over 600 technical publications on electronics packaging, with over 15,000 citations and an H-Index of 63 on Google Scholar. He has advised over 100 graduate students at Auburn University including over 40 PhD students working in the electronics industry and academia. He is a Fellow of ASME, Senior Member of IEEE, and member of SMTA and IMAPS. Dr. Suhling has been a member of the IEEE Electronics Packaging Society for the past 35 years, and is serving as Society President for a two-year term in 2026-2027. He received the EPS William Chen Distinguished Service Award in 2024.

Abstract: Electronics packaging is a field in rapid evolution due to strong and competing customer demands for increased functionality and performance, further miniaturization, heightened reliability, and lower costs. Such product drivers cause a myriad of reliability challenges for the engineer involved in the mechanical design of electronic systems. Accordingly, advanced experimental techniques are in high demand, and several methods of experimental solid mechanics have become critical tools for design and development of electronic products. In this short course, a presentation is made of most important and widely adopted experimental techniques that are applied to packaging for measurements of stress, strain, and deformation including

(1) Silicon Test Chips with Stress and Temperature Sensors;
(2) Scanning Acoustic Microscopy (CSAM);
(3) Digital Image Correlation (DIC);
(4) Optical methods for Characterization of Warpage;
(5) Moiré and Interferometric Techniques;
(6) Micromechanical Characterization of Solders, Underfills, and Thin Films.

To begin the course, the mechanics and reliability issues for modern electronic systems will be reviewed, and the challenges facing the experimentalist in the packaging field discussed. For each experimental method, discussion will be given of the theoretical fundamentals and equations that form the basis of the technique, as well as of the practical approaches and "tricks of the trade" needed by the experimentalist for successful implementation to advanced electronic packages and assemblies. Designs for specialized instruments and testing systems based on these methods will also be shown. Finally, a comparison of the capabilities of the various methods will be made as well as identifying the best techniques for various applications. Several case studies will be presented.