ICEPT2026 Empyrean

Workshop: EDA for Advanced Packaging & System Integration

Date: Friday, August 5th, 2026, 13:00-16:20 **Location**: Xi'an, China

Chair: Prof. Jun YANG, Southeast University **Dr. Michael lIU**, Empyrean

Driven by HPC and AI chips, Chiplet, 2.5D/3D IC and high-density SiP packaging have enabled continuous Moore's Law scaling. However, traditional EDA flows cannot support modern heterogeneous integration, creating critical gaps in multi-die co-design, multi-physics verification and manufacturability optimization. This session explores advanced packaging EDA innovations, bridging academic algorithms and industrial practices to cover STCO, physical optimization, multi-physics verification, DFM and AI-driven design automation.

Attendees gain access to cutting-edge technical insights, face-to-face exchanges with top EDA, OSAT and academic experts, and networking opportunities to foster cross-industry collaboration on domestic advanced packaging EDA ecosystem development.

EDA for Advanced Packaging & System Integration Session	
Sponsor: Empyrean	
Chair: Prof. Jun YANG, Southeast University	
13:00-13:10	***Welcome Address***
13:10-13:35	**Bridging PCB and Advanced Packaging: Our Journey Toward Package-Aware Design**
	Mr. Liang JIA*, Director in Semiconductor BU, Huatek*
13:35-14:00	**Advanced Packaging Design & Simulation Solutions and Challenges**
	Dr. Guangchao LV*, Senior R&D Engineer of National Center for Advanced Packaging Co., Ltd*
14:00-14:25	**Trends and Industrial Practices of STCO-Driven 3DIC Design Methodology**
	Dr. Michael LIU*, Product Director of Empyrean Technology Co., Ltd*
14:25-14:35	*Tea Break & Networking*
Chair: Xiaoming LIU, Empyrean	
14:35-15:00	***Physically Aware Logic Synthesis in the AI Era***
	Dr. Keren ZHU*, Assistant Professor of Fudan University*
15:00-15:25	**EDA Co-Simulation and Optimization for Structural Reliability Across the Full Chip Lifecycle: Chip Design, Packaging, System Integration, and Reliability Verification**
	Mr. Jian Cheng*, Expert Engineer, JCET*

15:25-15:50	**Thermal Simulation of Chiplet heterogeneous Integration system**
	Dr. Qinzhi XU, *Research Professor of Institute of Microelectronics of Chinese Academy of Sciences*
15:50-16:20	Panel

Introduction of Speaker

Bridging PCB and Advanced Packaging: Our Journey Toward Package-Aware Design

Liang JIA, Director in Semiconductor BU, Huatek

Speech Description/Objective: Bridging PCB and Advanced Packaging: Our Journey Toward Package-Aware Design explores the evolution of PCB design methodologies toward advanced packaging and heterogeneous system integration. As chiplet architectures, high-bandwidth memory (HBM), and UCIe-based interconnects reshape system design, traditional PCB-centric EDA tools are increasingly insufficient to address multi-die, high-density, and cross-domain integration challenges.

This presentation shares practical insights from extending a PCB design platform toward package-aware capabilities, including Flip-Chip and Wire Bond support, as well as emerging modeling requirements for micro-bumps, RDL, and hierarchical interconnect structures. It highlights key architectural changes required to move from flat board-level design toward hierarchical, system-level representation.

Introduction of Speaker: A software engineering professional with extensive experience in EDA software development, test engineering, and semiconductor manufacturing workflows. Since graduating in 2007, has worked across software development, test program design, and tester engineering platform integration, with solid expertise in PCB design tools and end-to-end manufacturing processes.

Currently responsible for the development and product direction of a PCB design software platform, driving its evolution toward advanced packaging and heterogeneous system integration capabilities. Key focus areas include support for Flip-Chip and Wire Bond design, as well as advanced packaging requirements such as multi-die connectivity, micro-bump and RDL modeling, and high-density interconnect optimization.

Current work emphasizes bridging traditional PCB design methodologies with emerging advanced packaging technologies, enabling the transition toward system-level electronic design platforms that support chip-package-board co-design under a unified data and architecture framework.

Advanced Packaging Design & Simulation Solutions and Challenges

Guangchao Lv, Senior R&D Engineer of National Center for Advanced Packaging Co., Ltd

Speech Description: As AI computing power demand surges and chip process scaling slows, advanced packaging has become a core path for system performance enhancement in the post-Moore era. This presentation will explore how system integration trends drive the rapid evolution of 2.5D/3D packaging technologies and share NCAP's practices in the full design-simulation-verification workflow of its one-

stop advanced packaging service platform. We will highlight key capabilities such as PDK-based co-design methodologies, signal and power integrity simulation optimization, and wafer-level warpage control. In addition, we will address major challenges including high-speed interconnects, integrated power delivery and thermal management, and multiphysics co-simulation. Finally, we will discuss how collaborative innovation across system, process, and design can accelerate the iteration and deployment of high-performance chip products.

Introduction of Speaker: Dr. Guangchao Lv currently serves as a Senior R&D Engineer at the National Center for Advanced Packaging Co., Ltd. (NCAP China). His primary research and engineering practice focus on advanced packaging structure design, reliability analysis, and design simulation.

Trends and Industrial Practices of STCO-Driven 3DIC Design Methodology

***Dr. Michael Liu**, Product Director of Empyrean Technology Co., Ltd*

Speech Description: In the post-Moore era, the traditional transistor miniaturization roadmap is approaching fundamental physical limits, making chiplet-based systems a critical solution to break through the bottlenecks of chip performance and cost. Driven by the evolving trends of semiconductor technology, this presentation systematically sorts out the evolutionary logic and future development directions of the STCO design methodology. It thoroughly analyzes the technical transition trajectory spanning from 2.5D integration to 3DIC, as well as the core transformations and inherent connotations behind the upgrade of design methodologies from DTCO to STCO. Combined with industrial implementation practices, this talk also introduces domestic end-to-end design flows for 2.5D chiplets and 3DIC, demonstrating the implementation pathway of advanced packaging and co-design of entire systems amid indigenous innovation of domestic EDA tools.

Introduction of Speaker: Michael Liu is the senior product director of Empyrean Technology. He has more than 10 years of experience in ASIC chip design, manufacturing, and packaging EDA software product development and management, focusing on the planning, development, and promotion of EDA products. He helps Empyrean build up a mature Analog/Mixed-Signal design flow, and expand it to the fields of other full custom design such as flat panel display, signal chain, memory, RF and optoelectronics. He is building a reliability design methodology for design-manufacturing collaboration and a PPAC-oriented design-manufacturing-packaging collaborative design solution. The solutions are widely adopted by national and international leading design houses.

Physically Aware Logic Synthesis in the AI Era

Dr. Keren Zhu, Assistant Professor of Fudan University

Speech Description: As Moore's law slows, 3D integration and advanced packaging are key to continued scaling. Yet logic synthesis is still done in a 2D mindset, where key decisions are made before physical and packaging realities are known, leaving a wide gap between logic level estimates and post layout quality. This talk argues that synthesis must become physically aware, and increasingly 3D aware. I will present our AI driven work bridging synthesis and physical design: PigMap, a physically aware technology mapping framework, and PhyLS, a full stack physically aware synthesis platform. I will then look ahead to 3D, extending

these ideas to inter die partitioning, vertical interconnects, and thermal and packaging constraints, and share open challenges in co optimizing logic, layout, and packaging together.

Introduction of Speaker: Keren Zhu is an Assistant Professor at Fudan University. He received his Ph.D. from the University of Texas at Austin under Prof. David Z. Pan. His research lies at the intersection of EDA, AI, and chip design, with a focus on AI empowered circuit design and optimization. He has published over 60 papers in leading EDA venues and is a main developer of the open source analog layout tool MAGICAL. He serves on the technical program committees of DAC, ICCAD, GLVLSI, and MLCAD, and as IEEE CEDA Shanghai Chapter Chair. He was named to the MIT Technology Review Innovators Under 35 Asia Pacific list and selected for national level young talent programs.

EDA Co-Simulation and Optimization for Structural Reliability Across the Full Chip Lifecycle: Chip Design, Packaging, System Integration, and Reliability Verification

Mr.Jian Cheng, Expert Engineer, JCET

Speech Description:

This presentation focuses on EDA-driven co-simulation technologies for structural reliability throughout the entire chip lifecycle, covering the full development workflow from chip design and advanced packaging to system assembly and product reliability testing and verification. Closely aligned with the theme of this session, the talk will explore chip and system design optimization, closed-loop EDA design flows, as well as key pain points and engineering challenges in industrial-scale packaging manufacturing. The goal is to provide systematic methodologies and practical references for structural reliability design and verification of advanced packaged products.

Introduction of Speaker: Cheng Jian is an Expert Engineer in the Technology Service Department at JCET and the lead of the Structural Mechanics Testing and Simulation Platform. He holds a Master's degree in Chemical Process Machinery from Zhejiang University and is currently pursuing a part-time Ph.D. at the University of Electronic Science and Technology of China. He has long been engaged in research on the mechanical reliability of advanced chip packaging and systems. With 15 years of industrial R&D experience, he has published multiple papers as first/corresponding author at the top international packaging conferences including ECTC and ICPT, and holds multiple granted patents in China and abroad.

Thermal Simulation of Chiplet heterogeneous Integration system

Dr. Qinzhi Xu, Research Professor of Institute of Microelectronics of Chinese Academy of Sciences

Speech Description: As chip dimensions continue to scale down, chiplet-based heterogeneous integration has emerged as a pivotal approach for extending Moore’s law, yet it also introduces formidable thermal management challenges. In recent years, physics-informed neural networks (PINNs) have demonstrated promising potential for thermal simulation of integrated circuits; however, when applied to structures with complex geometries, they are prone to becoming trapped in local minima. In this work, we embed numerical computation methods into neural operator learning and propose a hybrid training framework that couples DeepONet with hard-constraint projection. This framework is further extended to the

thermal simulation of chiplet heterogeneous integration systems. By incorporating Latin hypercube sampling and grid-based sampling to strengthen physical constraints, high-fidelity temperature simulations of the chiplet system are realized. Numerical experiments confirm that the proposed method yields temperature predictions consistent with conventional numerical simulations while achieving a speedup of nearly 400×, underscoring the potential of physics-guided deep learning for thermal analysis of advanced electronic packaging.

Introduction of Speaker： Xu Qinzhi, Ph.D. and Professor and Doctoral Supervisor at the Institute of Microelectronics of Chinese Academy of Sciences (CAS). He has long been engaged in research on multiphysics simulation of three-dimensional integrated chips, design-for-manufacturability (DFM) methodologies for nanoscale chips, multiphysics modeling approaches for advanced device processes, structure–property relationships of nanocomposites based on first-principles calculations, and electronic design automation (EDA) software tools. He possesses extensive R&D experience in key simulation models for critical nanoscale chip processes and in EDA technologies for multiphysics simulation of integrated chips. He has proposed a coupled density functional theory (DFT) and integral equation simulation method for multi-site polymer nanocomposites, and developed a series of multiphysics simulation model engines for HKMG, FinFET, and copper-interconnect CMP processes, as well as a multiphysics simulation tool for chiplet integration system. He has undertaken nearly 30 projects funded by national programs, the Beijing municipal government, the Chinese Academy of Sciences, and industry collaboration initiatives, with related technological achievements successfully transferred to well-known enterprises. As the first author or corresponding author, he has published over 100 SCI papers, patents, and software copyrights. He has received awards including the Third Prize of the Beijing Municipal Science and Technology Award and the Second Prize of the Science and Technology Award of the Chinese Institute of Electronics.