From DIP to MIP: 40 years in semiconductor packaging

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Abstract:

Packaging of integrated circuits has gained considerable importance in product development since in 1982 the speaker joined Philips Semiconductors, now NXP, as corporate development manager. Starting at that time with the Dual-in-line Package (DIP) we are now at extremely complex multi-chip arrays like chiplets and 3D integrated systems. The trends to more Moore and more than Moore included many new packaging concepts, the introduction of new materials and ever increasing requirements, while always struggling with considerable power dissipation challenges. Many new applications came at the horizon like mobile, automotive and AI requiring advanced tools for reliability analysis. In this presentation we look back at 40 years packaging as experienced by the speaker ending with the MIP as a new tool, that was developed by us in 2014 and now having a wide range of applications in reliability analysis.

Speaker's Biography:

In 1974 Kees Beenakker joined Philips Research Laboratories in Eindhoven, the Netherlands, where he was involved in research on plasma systems for environmental analysis and microelectronics patterning. In 1982 he was the corporate assembly and packaging development manager at Philips Semiconductors establishing intensive contacts with the assembly factories in the Far East. In 1989 he was appointed chair professor at the Delft University and retired in 2014 as scientific director of the Delft Institute of Microelectronics and head of the department of Microelectronics. From 2006 till 2014 he held a honorary guest professorship at Tsinghua University. Based on his earlier work he invented the MIP as a tool for reliability analysis in microelectronics and established in 2014 together with Dr. Jiaqi Tang the Delft company Jiaco Instruments which he now serves as a member of the advisory board.