Flip Chip on Glass-Core Substrate with Micropump and Cu-Cu Hybrid Bonding

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Abstract:

In this lecture, two problems of flip chips on glass-core package substrate will be investigated. The first problem deals with the flip chip on glass-core package substrate with microbumps and the other deals with the flip chip on glass-core package substrate with Cu-Cu hybrid bonding. The first problem is for high-performance applications and the second problem is for very high-performance applications. For both cases there are two build-up layers on the glass-core’s top and bottom sides. For the microbumped flip chip the build-up layers are fabricated by a PID (photoimageable dielectric) for the dielectric layer (5µm-thick) and electrochemical deposition (ECD) Cu for the metal layer (3µm-thick). The pad pitch is 50µm. For comparison purposes, a same structure with organic-core package substrate with microbump is also considered. For Cu-Cu hybrid bonding flip chip, the build-up layers on the glass-core’s top and bottom sides are fabricated by PECVD (plasma-enhanced chemical vapor deposition) for the SiO_2 dielectric layer (1.5µm-thick) and Cu dual-damascene for the metal layer (1.5µm-thick). The Cu-pad pitch is 10µm. One of the key takeaways is to point out a common mistake that the thermal coefficient of expansion of the glass-core substrate is as close as that of the silicon chip. Some recommendations will be provided.

Speaker's Biography:

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 535 peer-reviewed papers (385 are the principal investigator), 52 issued and pending US patents (31 are the principal inventor), and 24 textbooks. John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.