PDC 1: Advanced packaging for High Performance Computing

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Outline:

1.Fast development of high performance computing chip driven by AI

2. Advanced packaging requirement for HPC

- Development of advanced packaging technology for HPC

1) TSV Interposer technology
2) Organic interposer technology
3) Bridge interconnect technology
4) Glass interposer and TGV substrate
5) CPO technology
6) High performance heat management)

3. Development trend and challenges for advanced packaging for HPC

4. Conclusion

Lecturer Biography:

In 2004, he studied at Dalian University of Technology and obtained a doctorate degree in engineering. He has carried out research work in internationally renowned research institutions such as City University of Hong Kong, Fürnhofer Institute for Reliability and Microintegration, and Singapore Institute of Microelectronics. From 2010 to 2015, he served as a researcher at the Institute of Microelectronics, Chinese Academy of Sciences. From 2014 to 2019, he served as the dean of the Packaging Technology Research Institute of Tianshui Huatian Technology Co., Ltd. In 2019, he served as the chairman of Yuntian Semiconductor and a distinguished

professor of Xiamen University. He serves as a distinguished expert of the overall group of the 02 special project of the National Science and Technology Major Project, the vice chairman of the MEMS Branch of the China Semiconductor Industry Association, a member of the National Technical Committee for Standardization of Semiconductor Devices, and a senior member of IEEE. He has been selected into the "Hundred Talents Program" of the Chinese Academy of Sciences, the "Hundred Talents Program" of Xiamen City and Fujian Province. He has presided over many national major science and technology projects 02 projects and topics, published more than 200 academic papers, authorized more than 70 national invention patents, and won the first prize of the 2020 National Science and Technology Progress Award.